普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT2399 is an echo audio processor IC utilizing CMOS Technology which is equipped with ADC and DAC, high sampling frequency and an internal memory of 44K Digital processing is used to generate the delay time, it also features an internal VCO circuit in the system clock, thereby, making the frequency easily adjustable. PT2399 boast of very low distortion (THD<0.5%) and very low noise (No<-90dBV), thus producing high quality audio output. The pin assignments and application circuit are optimized for easy PCB layout and cost saving advantage.

FEATURES

- CMOS Technology
- Least External Components
- Auto Reset Function
- Low Noise, No<-90dBV Typical
- Low Distortion, THD<0.5% Typical
- External Adjustable VCO
- Available in 16 pins, DIP or SOP

APPLICATIONS

- Video Tape Recorder
- Video Compact Disk
- Television
- CD Player
- Car Stereo
- KARAOKE Mixer
- Electronic Musical Instrument
- Audio Equipment with Echo Processor

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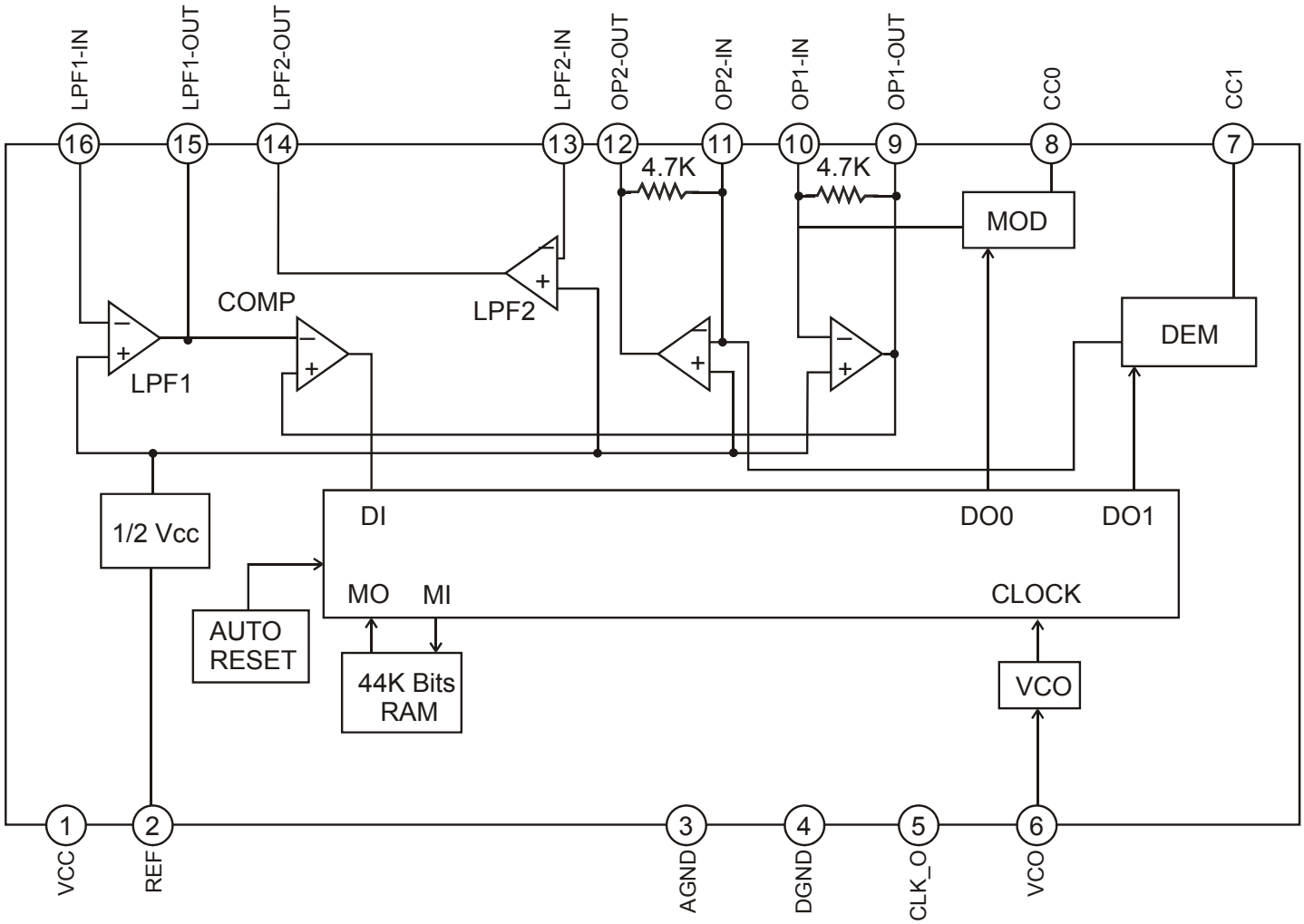
BLOCK DIAGRAM



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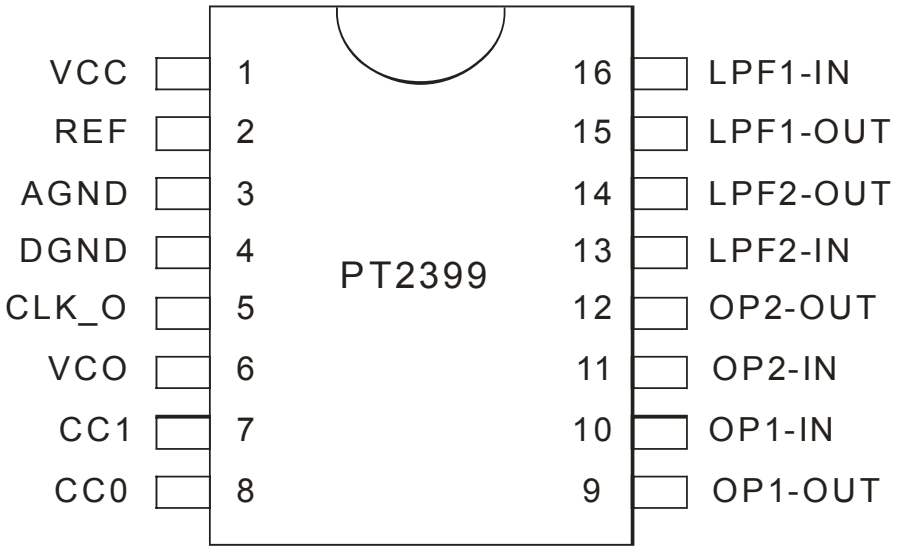
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VCC	-	Analog Supply Voltage Input	1
REF	-	Analog Reference Voltage (1/2VCC)	2
AGND	-	Analog Ground	3
DGND	-	Digital Ground	4
CLK_O	O	System Clock Output Pin	5
VCO	I	Frequency Adjustment Pin	6
CC1	-	Current Control 1	7
CC0	-	Current Control 0	8
OP1-OUT	O	OP Amplifier 1 Input/Output, This pin can be used as Modulated/Demodulated Integrator by connecting Capacitor	9
OP1-IN	I		10
OP2-IN	I	OP Amplifier 2 Input/Output, This pin can be used as Modulated/Demodulated Integrator by connecting Capacitor	11
OP2-OUT	O		12
LPF2-IN	I	Low Pass Filter 2 Input/Output Pin	13
LPF2-OUT	O		14
LPF1-OUT	O	Low Pass Filter 1 Input/Output Pin	15
LPF1-IN	I		16

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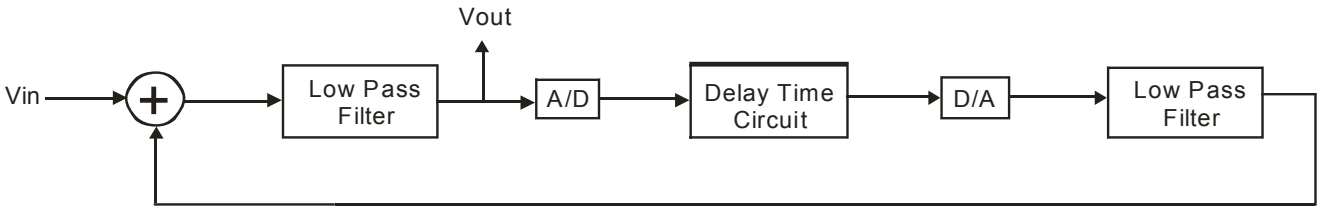
FUNCTION DESCRIPTION

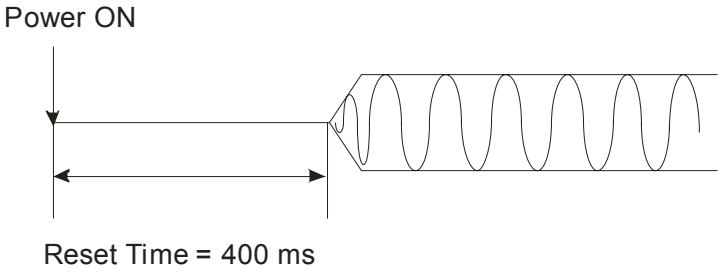
ECHO MODE

Please refer to the diagram below:



AUTO RESET FUNCTION

The waveform of the signal during power on is given below:



ABSOLUTE MAXIMUM RATING

(Unless otherwise specified, Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	6.5	V
Supply Current	Icc	100	mA
Power Dissipation	Pd	1.7	W
Operation Temperature	Topr	-40 to +85	℃
Storage Temperature	Tstg	-65 to +150	℃

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	5	5.5	V
Clock Frequency	fck	-	4	5	MHz

AC CHARACTERISTICS

(Unless otherwise specified: Vcc=5.0V, fin=1KHz, Vi=100mVrms, fck=2MHz, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	-	4.5	5.0	5.5	V
Supply Current	Icc	-	-	30	40	mA
Voltage Gain	Gv	RL=47KΩ	-	-0.5	2.5	dB
Max. Output Voltage	Vomax	THD=10%	1.5	2	2.5	Vrms
Output Distortion	THD	filter=A-weighting	-	0.3	1.0	%
Output Noise Voltage	No	filter=A-weighting	-	-90	-80	dBV
Power Supply Rejection Ratio	PSRR	ΔVcc=-20dBV(0.1Vrms), f=100Hz	-	-40	-30	dB

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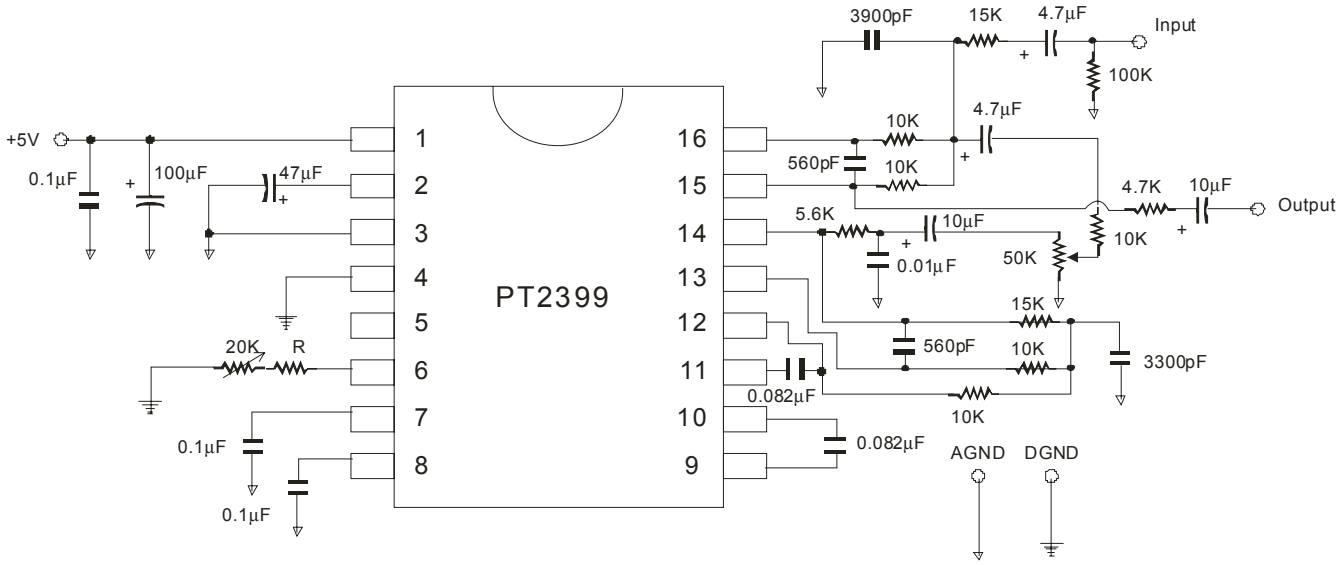
APPLICATION CIRCUIT

ECHO



Note:
External Resistor having a value of 10 KΩ to 50 KΩ may be used. The recommended Resistor Value(R) is 10 KΩ. When the value of the Resistor (R) increases, the range of the Delay Time also increases.

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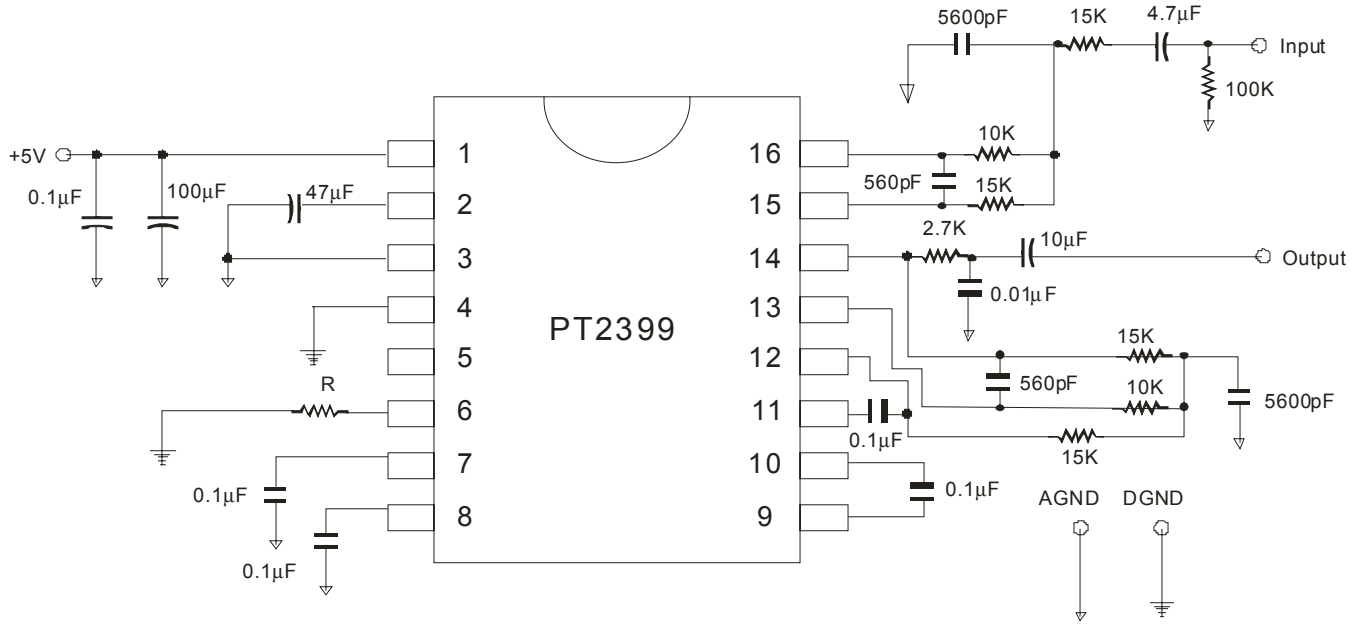
SURROUND/DELAY



Note: Please refer to Table 1 for the Resistor/Delay Time values.

TABLE 1: RESISTOR/DELAY TIME VALUES

R	27.6K	21.3K	17.2K	14.3K	12.1K	10.5K	9.2K	8.2K
fck	2.0M	2.5M	3.0M	3.5M	4.0M	4.5M	5.0M	5.5M
td	342ms	273ms	228ms	196ms	171ms	151ms	136.6ms	124.1ms
THD	1.0%	0.8%	0.63%	0.53%	0.46%	0.41%	0.36%	0.33%

R	7.2K	6.4K	5.8K	5.4K	4.9K	4.5K	4K	3.4K
fck	6.0M	6.5M	7.0M	7.5M	8.0M	8.5M	9.0M	10M
td	113.7ms	104.3ms	97.1ms	92.2ms	86.3ms	81ms	75.9ms	68.1ms
THD	0.29%	0.27%	0.25%	0.25%	0.23%	0.22%	0.21%	0.19%

R	2.8K	2.4K	2K	1.67K	1.47K	1.28K	1.08K	894
fck	11M	12M	13M	14M	15M	16M	17M	18M
td	61.6ms	56.6ms	52.3ms	48.1ms	45.8ms	43ms	40.6ms	38.5ms
THD	0.18%	0.16%	0.15%	0.15%	0.15%	0.15%	0.14%	0.14%

R	723	519	288	0.5
fck	19M	20M	21M	22M
td	36.6ms	34.4ms	32.6ms	31.3ms
THD	0.14%	0.13%	0.13%	0.13%

Note:
1. R = External Resistor (Ω), please refer to PT2399 Surround/Delay Time Application Circuit.
2. fck = Clock Frequency (Hz).
3. td = Delay Time
4. THD = Total Harmonic Distortion

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ORDER INFORMATION

Part Number	Package Type	Top Code
PT2399	16 Pins, DIP, 300mil	PT2399
PT2399S	16 Pins, SOP, 300mil	PT2399S
PT2399-SN	16 Pins, SOP, 150mil	PT2399-SN
PT2399 (L)	16 Pins, DIP, 300mil	PT2399
PT2399S (L)	16 Pins, SOP, 300mil	PT2399S
PT2399-SN (L)	16 Pins, SOP, 150mil	PT2399-SN

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

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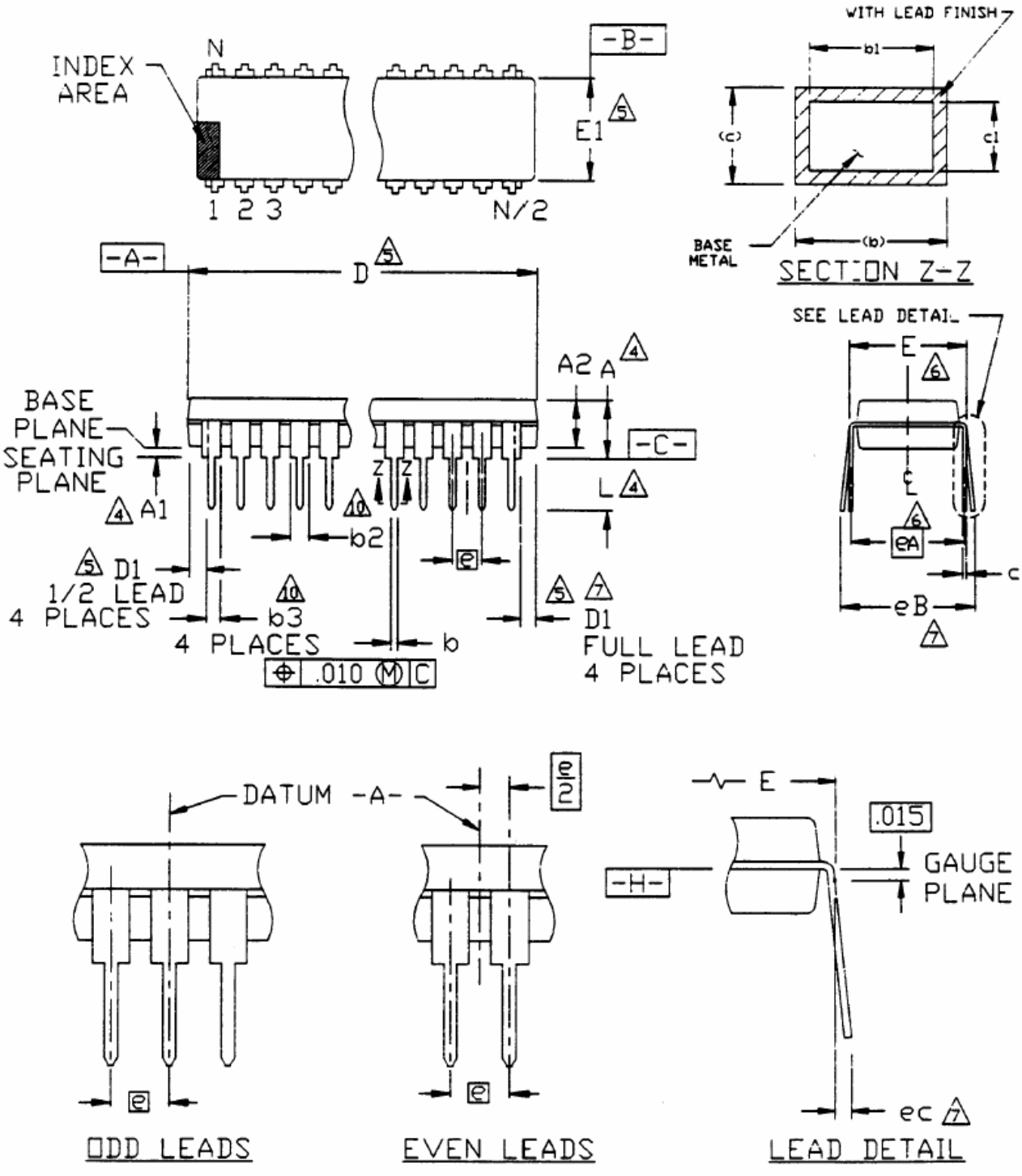
PACKAGE INFORMATION

16 PINS, DIP, 300 MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.780	0.790	0.800
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 BSC.		
eA	0.300 BSC.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. Controlling Dimension: INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions “A”, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D, “D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -C-.
6. “eB” and “eA” are measured at the lead tips with the leads unconstrained.
7. N is the maximum number of terminal positions (N=16).
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25mm).
10. Variation AB is a full lead package.
11. Distance between leads including dambar protrusions to be 0.005 in minimum.
12. Datum plane -H- coincident with the bottom of lead where lead exits body.
13. Refer to JEDEC MS-001 Variation AB.

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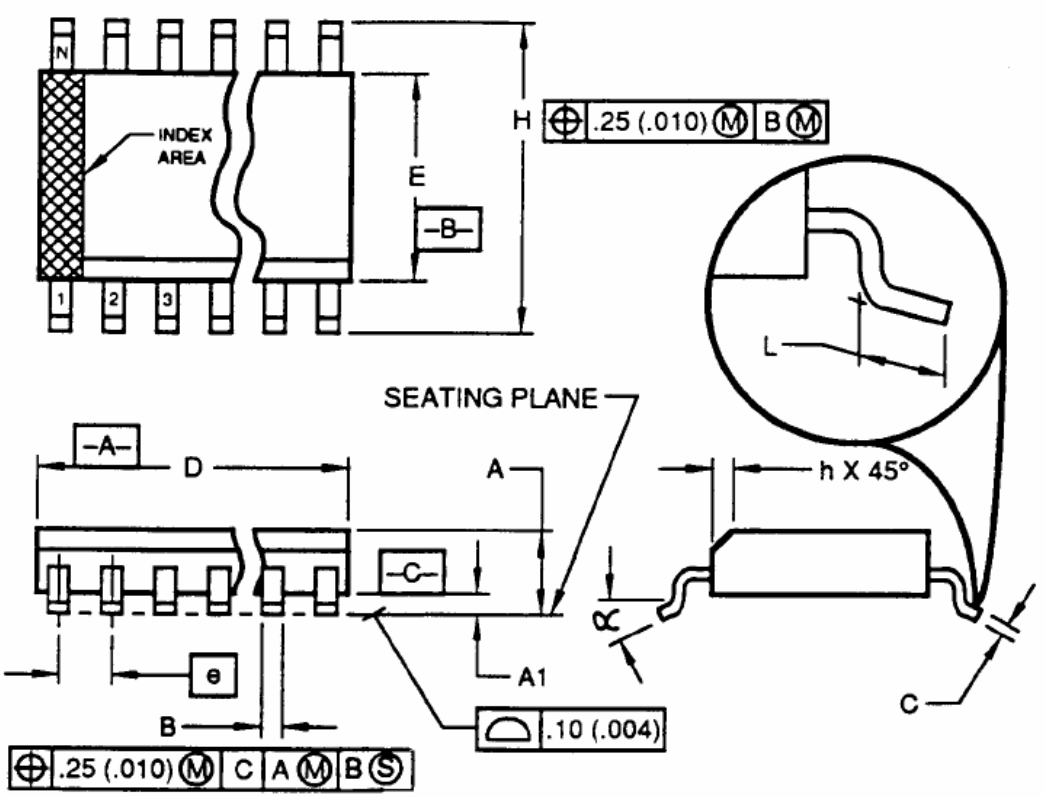
16 PINS, SOP, 300 MIL



Symbol	Min.	Max
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	10.10	10.50
E	7.40	7.60
e	1.27 BSC.	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0^o	8^o

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Notes:
1. Controlling Dimension: MILLIMETER
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 in) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25 mm (0.010 in.) per side
5.. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area
6. L is the length of the terminal for soldering to a substrate.
7. N is the number of terminal positions (N=16).
8 The lead width B, as measured 0.36 mm (0.014in) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024in.)
9. Refer to JEDEC MS-013 Variation AA.

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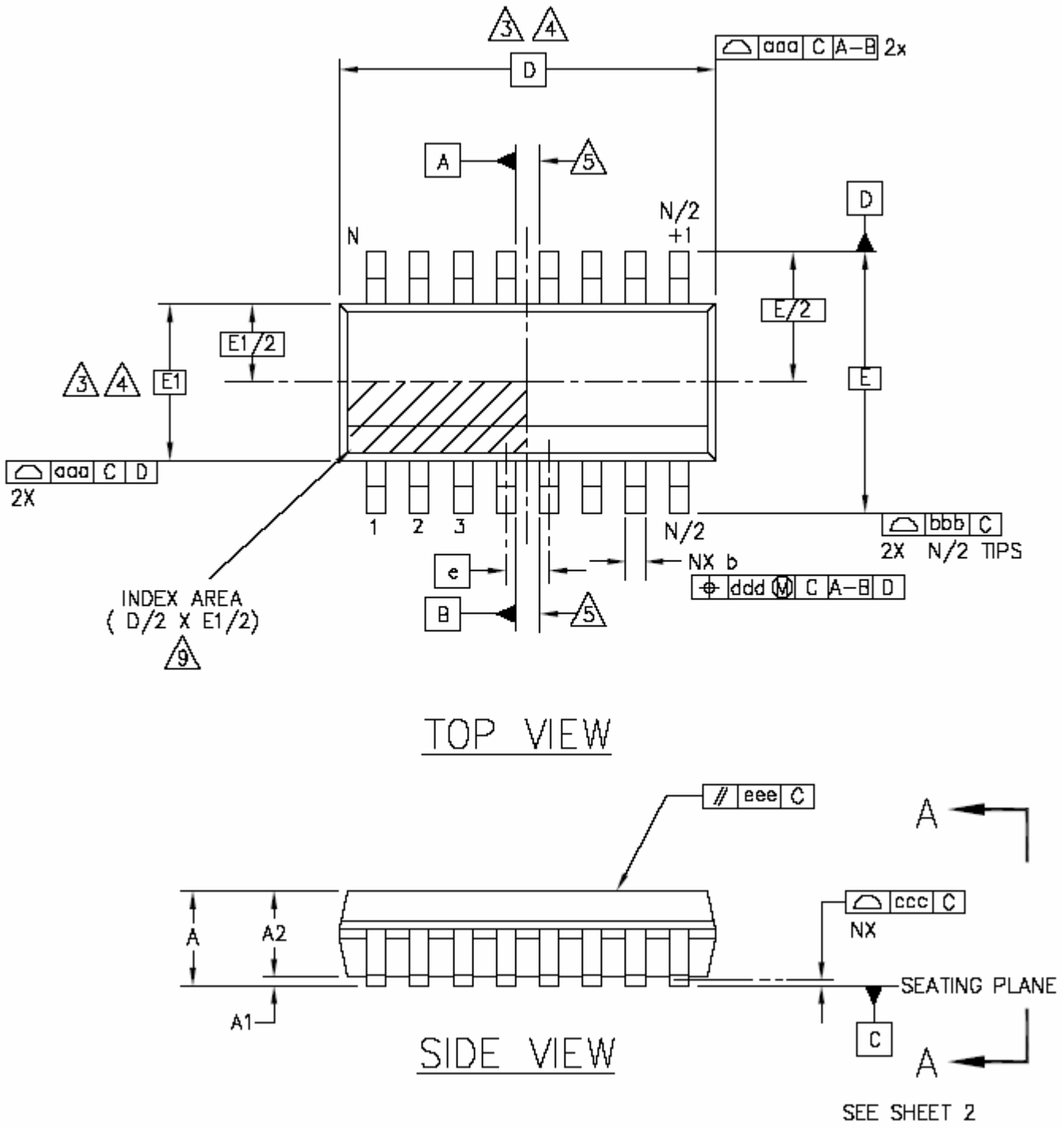
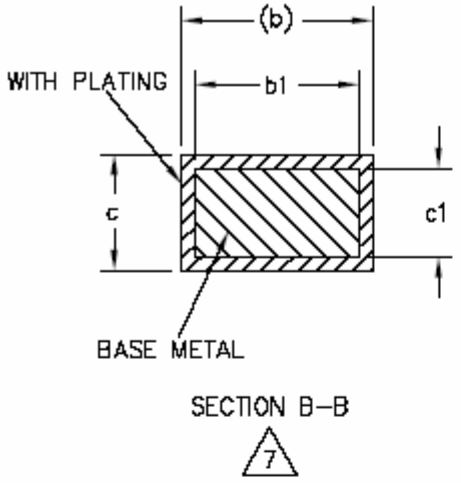
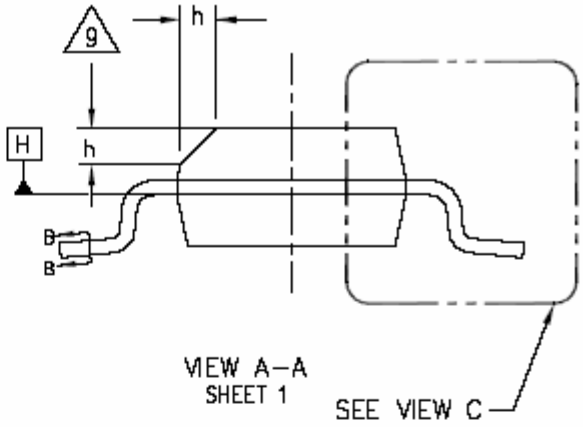
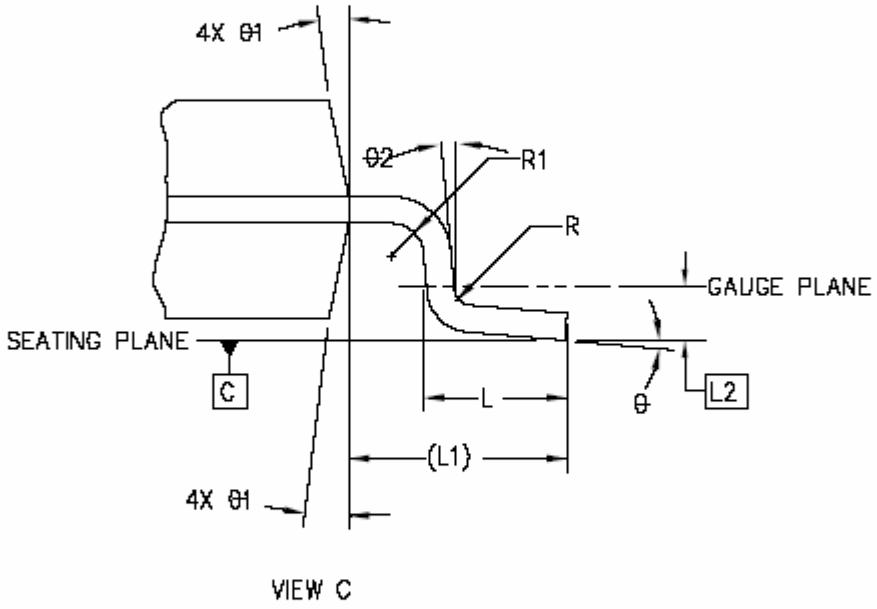
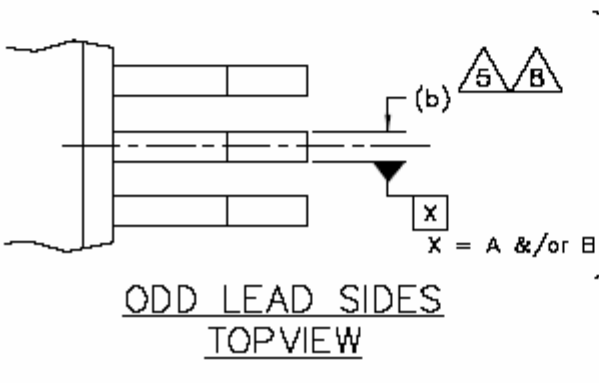
16 PINS, SOP, 150MIL

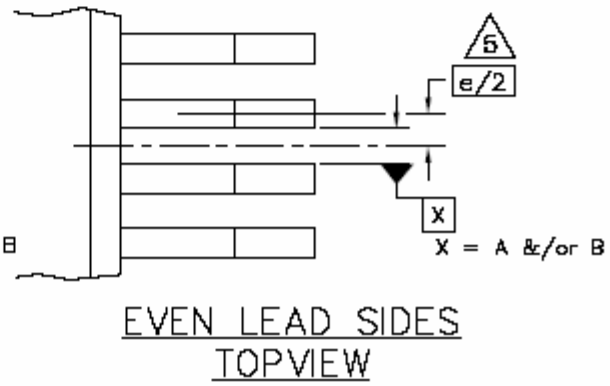



(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7


9
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C


4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C


(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW


5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	9.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Note:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AC.

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